Thermal aspects in electronic hardware design

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Electronic design trends

Faster (and faster) data transfer

Wired

Wireless

Faster processing

Complex processors

FPGA

System-on-Chip

Small footprints

BGA

QFP

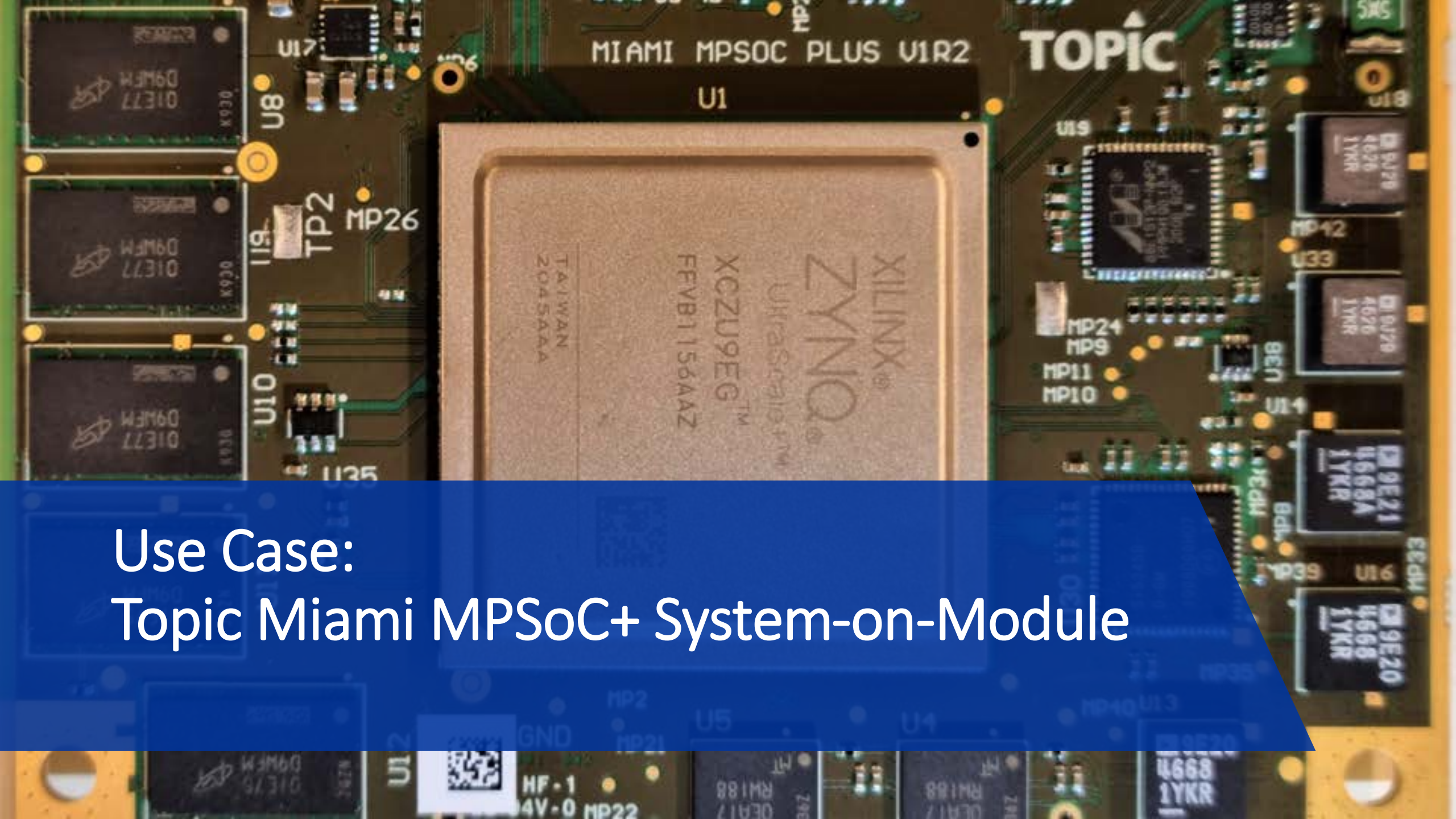
Small PCB

Multi-layer

HDI

Thermal Contributors

- High-speed Switching
- Processors and FPGAs
- Communication phys (Ethernet)
- Component power consumption
- Power plane resistance



Use Case:
Topic Miami MPSoC+ System-on-Module

Customer requests

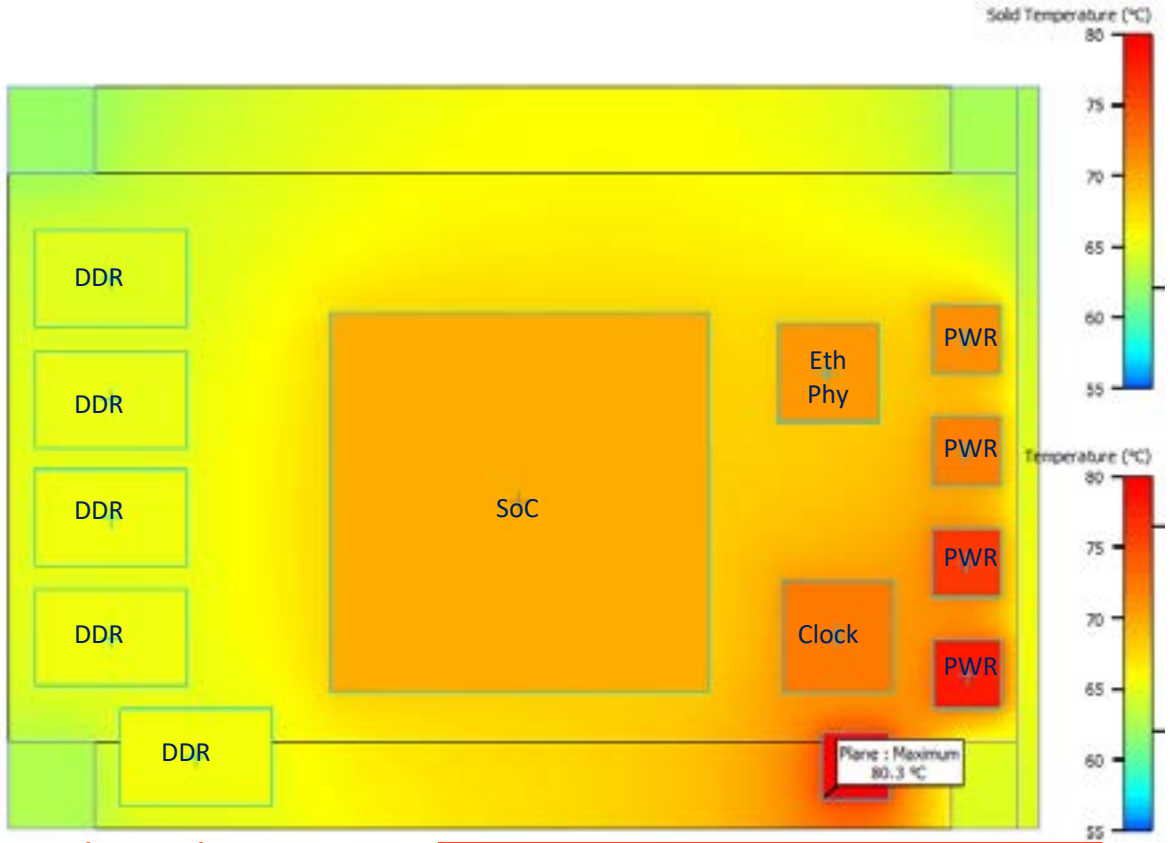
- Environmental conditions: -40 to +85 ˚C (storage -55 to +85 ˚C)
- Synchronous 1G Ethernet
- 16x high-speed transceivers (12-16Gbps)
- Very demanding processor and FPGA logic load
- Consumption up to 50W @ 55 ˚C
- Consumption up to 30W @ 85 ˚C
- 8GB DDR4 memory
- Small formfactor (95 x 70 mm)
- Low component height
- Limited cooling

Design considerations

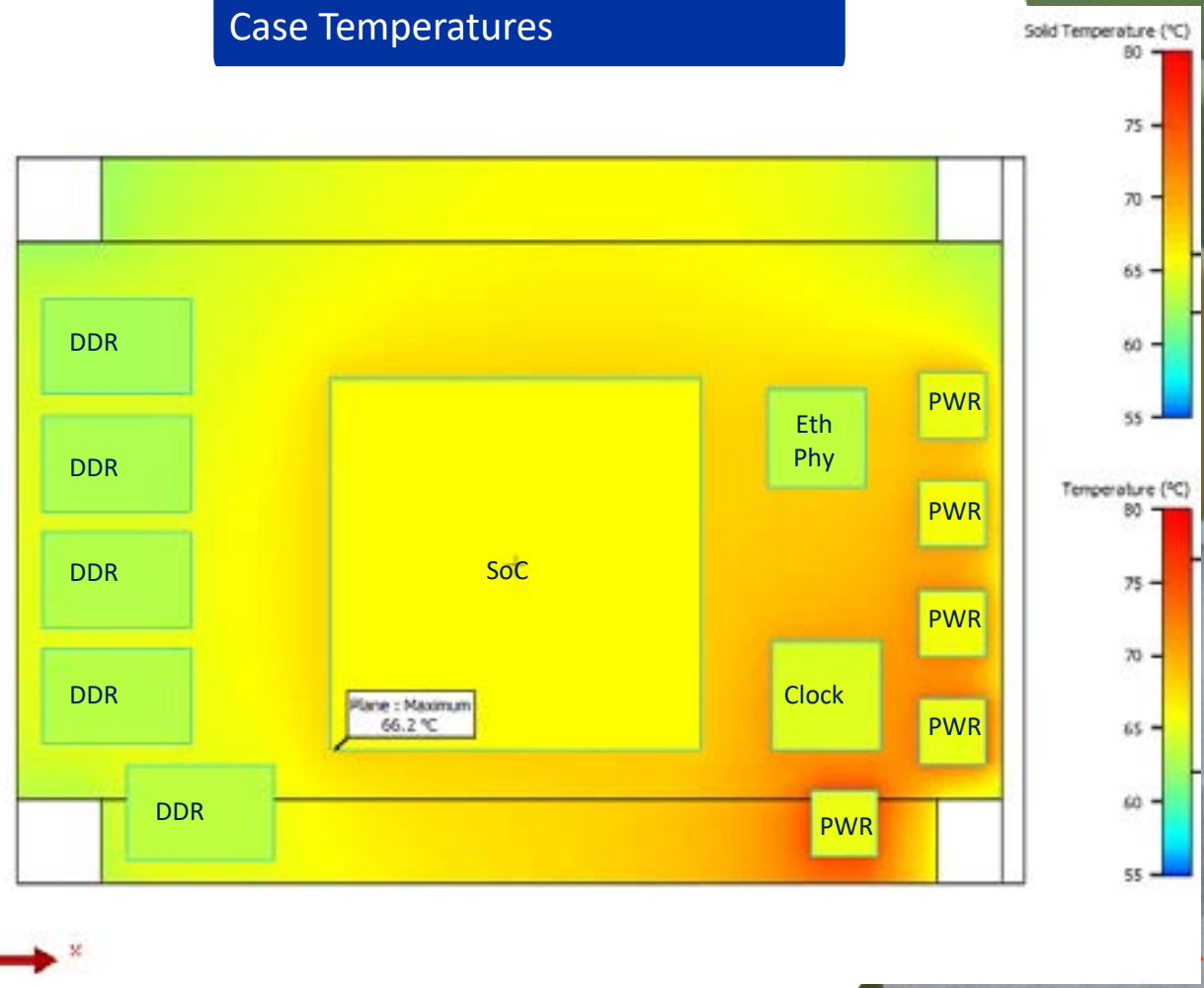
- Component choices
  - Heat conduction into PCB
- PCB
  - Number and thickness of layers
  - Stack-up
  - Copper coverage per layer
  - Thermal provisions
    - Vias
    - Mounting holes
    - Exposed copper
  - Special construction – Side plating
- Heatsink design

Component thermal simulations (55˚C) – 30W

Junction Temperatures

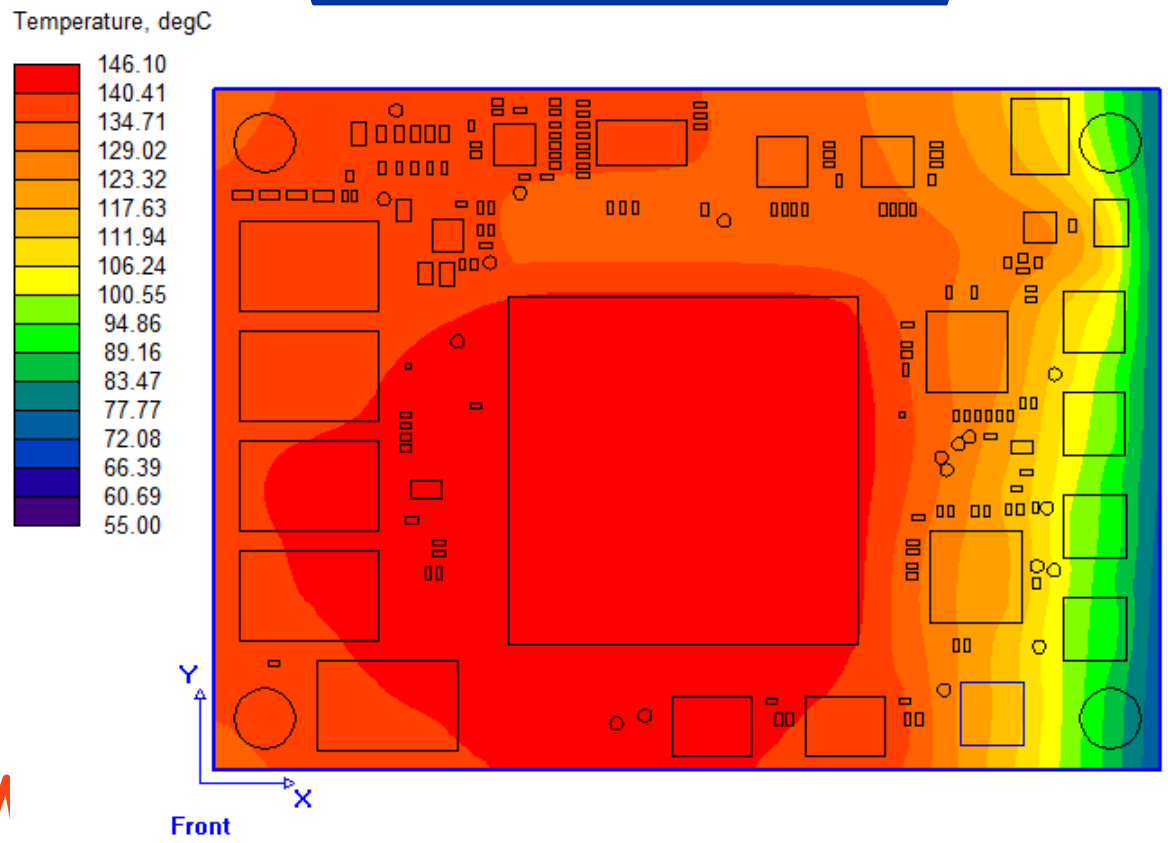


Case Temperatures

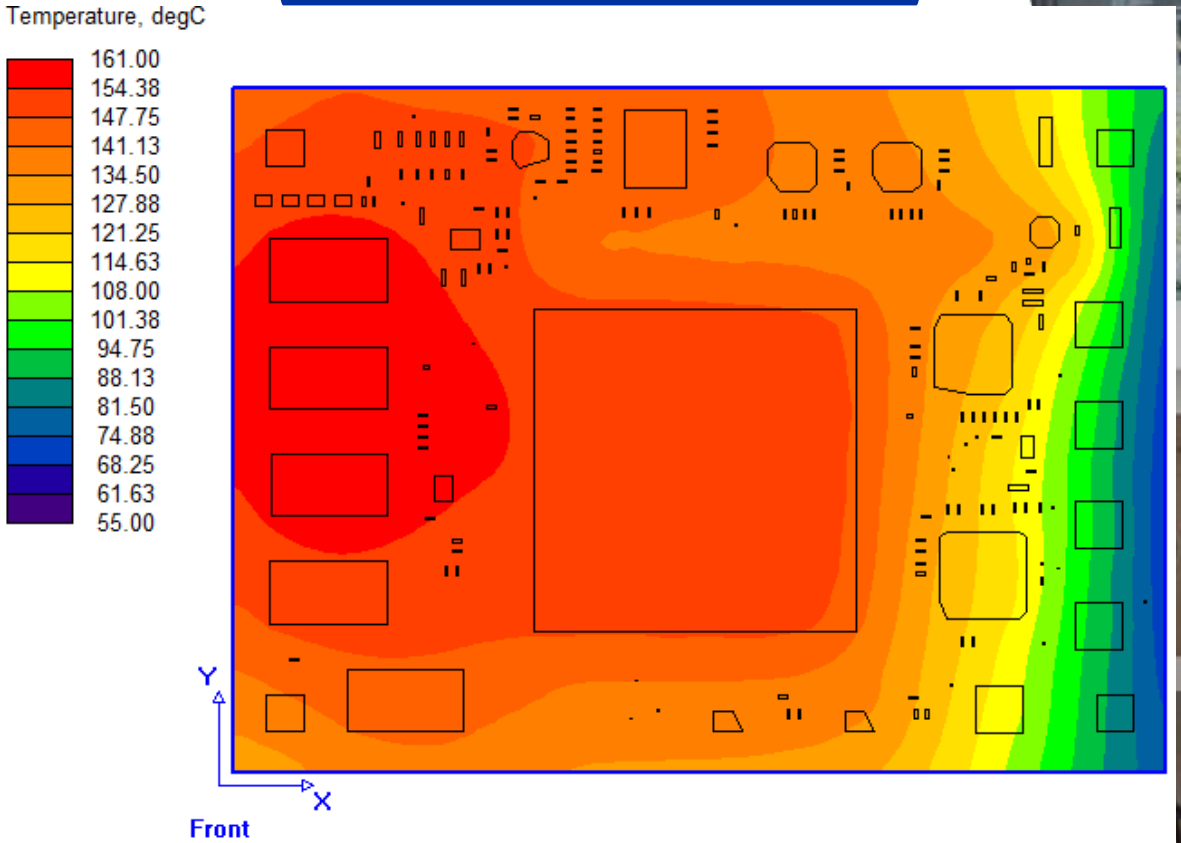


PCB Thermal distribution (55˚C) – 30W without heatsink

Version 1



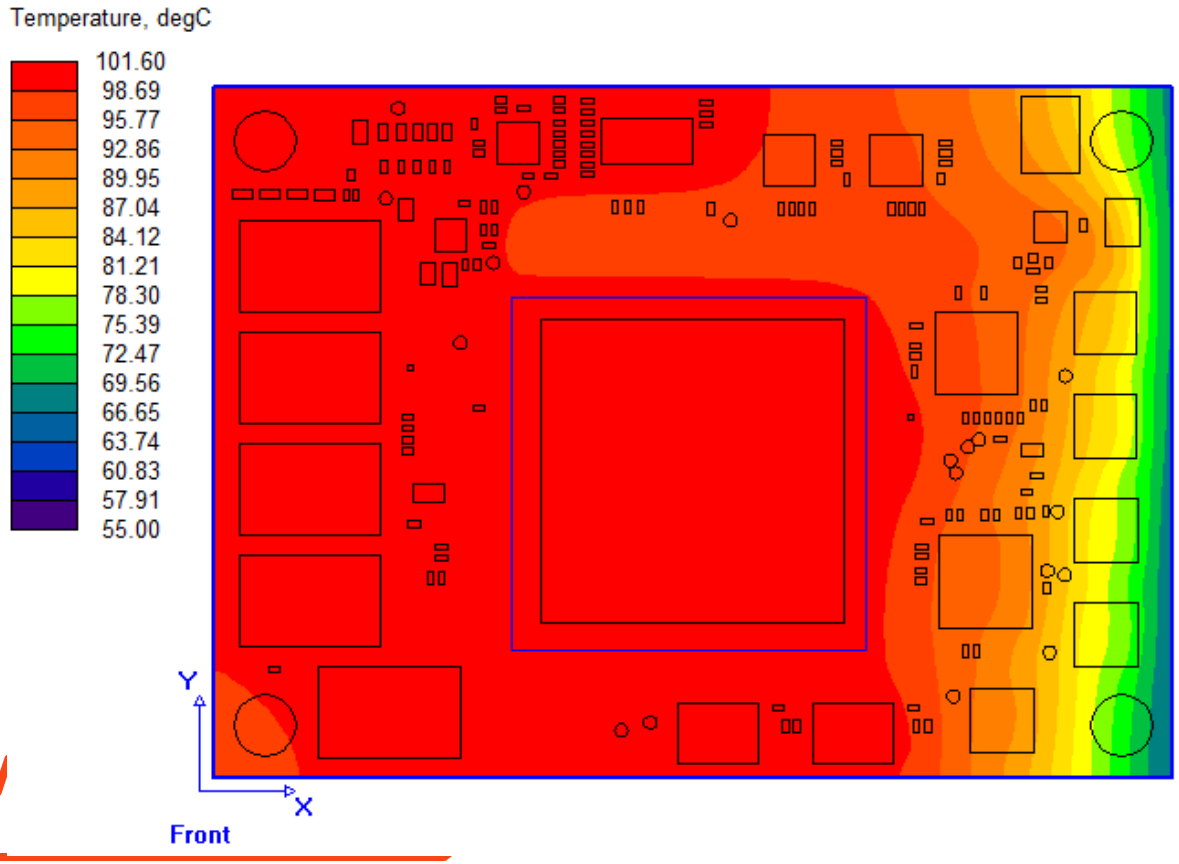
Version 2



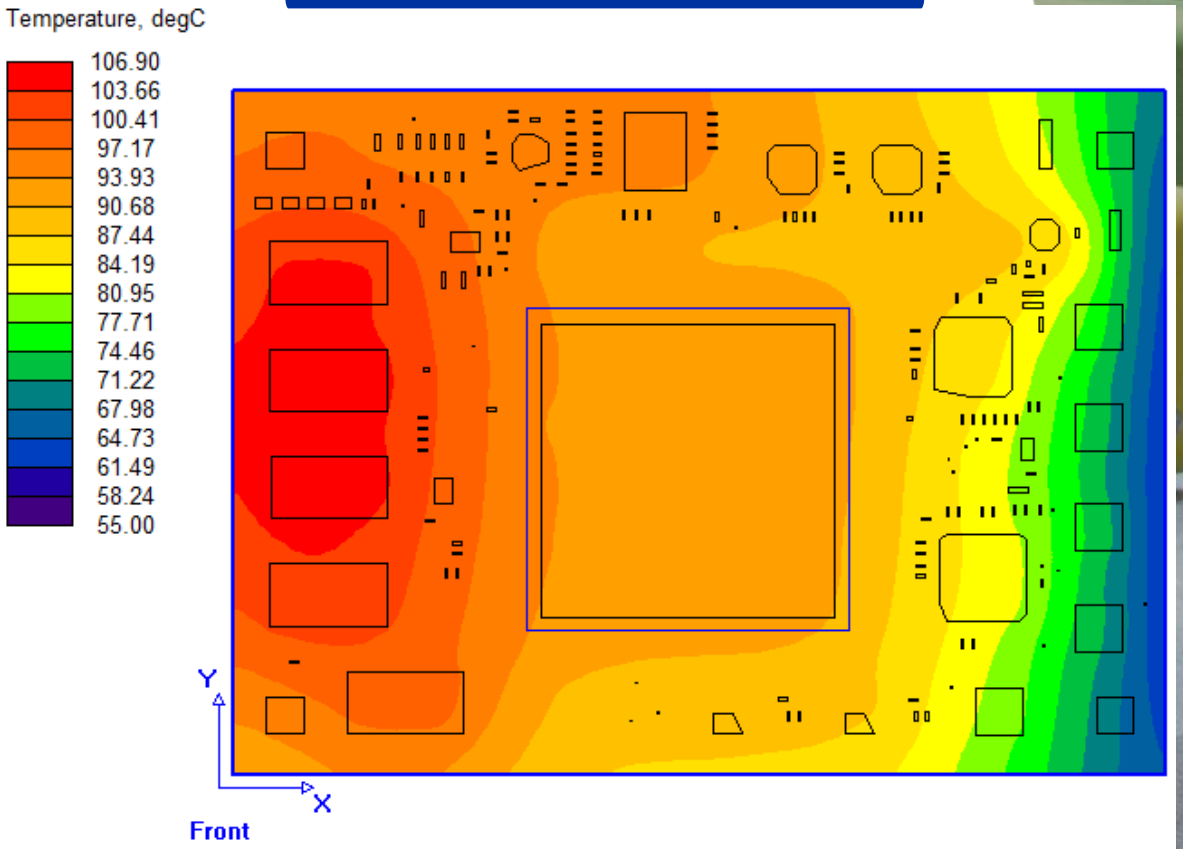
PCB Thermal distribution (55 °C) – 30W with heatsink on SoC

TOPIC

Version 1

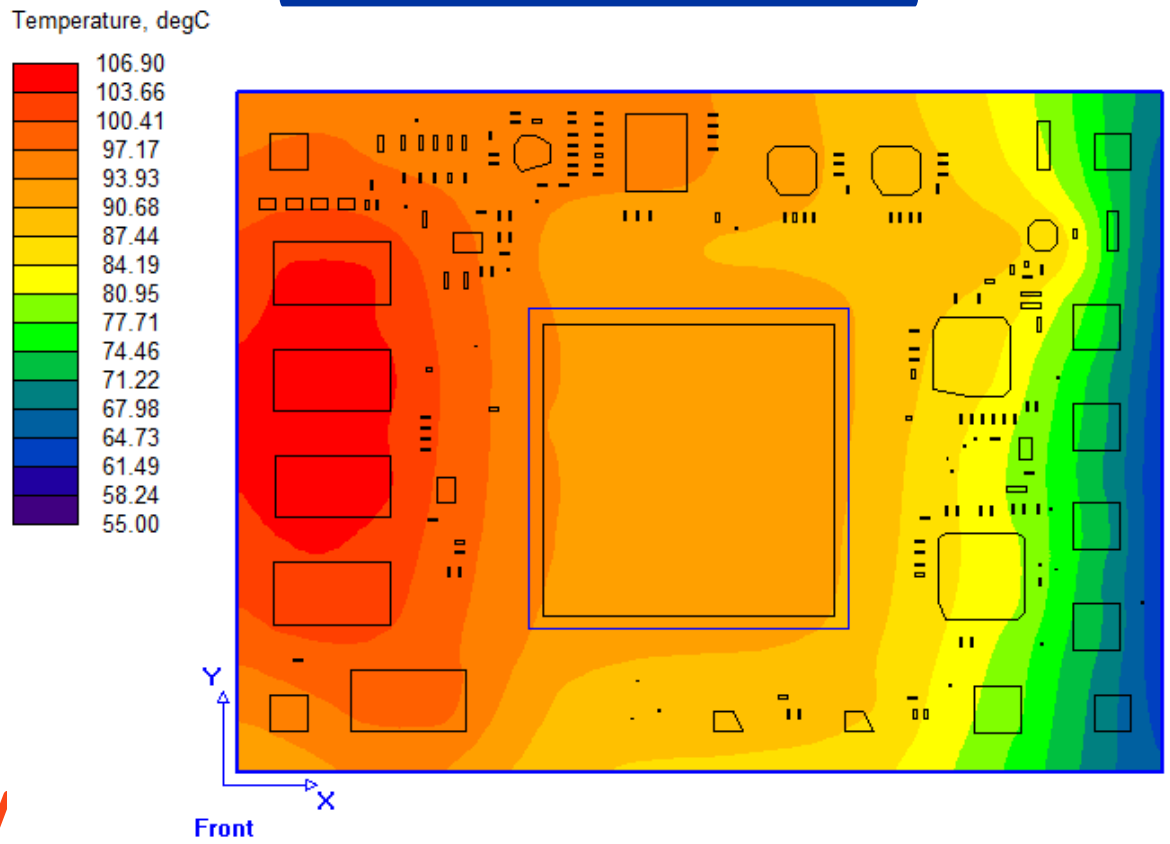


Version 2

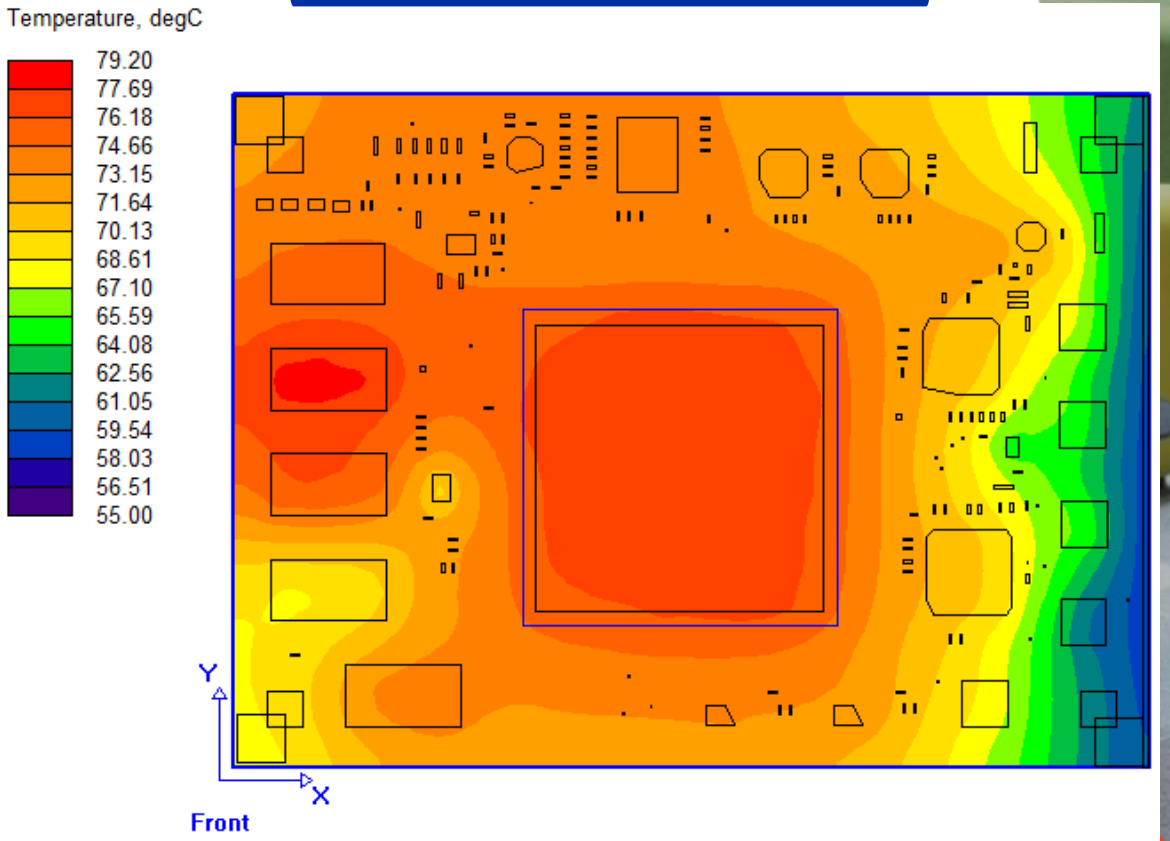


Thermal distribution (55˚C) – 30W with heatsink on SoC, PCB Edge and conducting mounting holes

Version 2 – Heatsink (SoC only)



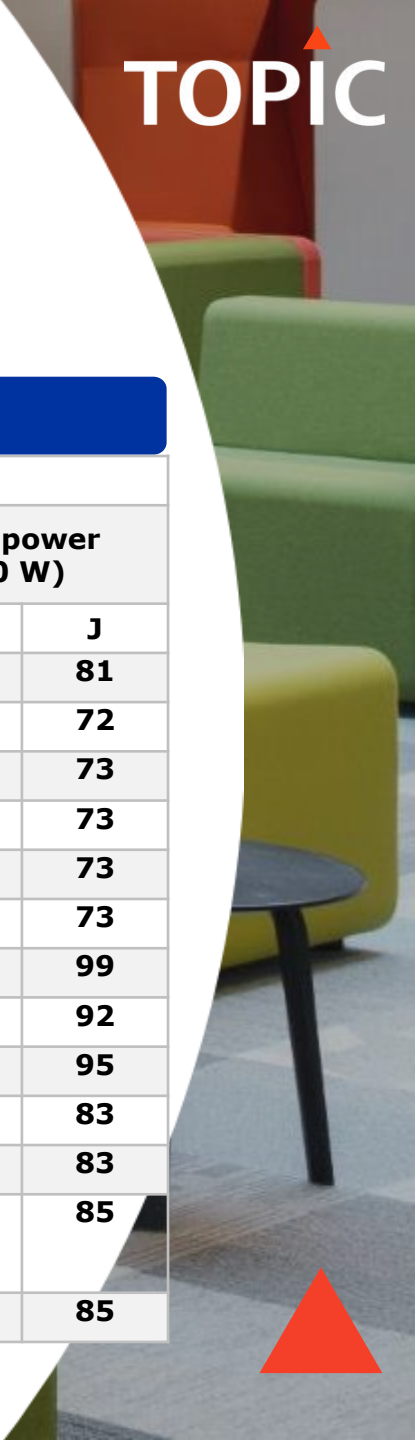
Version 2



Board thermal simulations parameter with heatsink on SoC, PCB Edge and mounting holes – 55˚C

Simulated Component Temperatures

Component	Description	Temperature, °C							
		Max operating junction	Low power (10 W)		Low nominal (20 W)		Nominal (29 W)		High power (50 W)	
			C	J	C	J	C	J	C	J
U1	FPGA	100	59	60	63	65	66	70	74	81
U8	DDR4	100	58	58	60	62	63	65	68	72
U9	DDR4	100	58	59	61	62	63	65	69	73
U10	DDR4	100	58	59	61	62	63	66	69	73
U11	DDR4	100	58	59	61	62	63	66	69	73
U12	DDR4	100	58	59	61	62	63	66	69	73
U13	DC/DC Reg	125	59	64	62	72	65	80	73	99
U14	DC/DC Reg	125	59	62	62	70	66	76	74	92
U16	DC/DC Reg	125	59	63	62	71	65	78	73	95
U18	DC/DC Reg	125	59	61	62	66	65	71	73	83
U19	Ethernet Phy	125	58	61	61	66	64	71	70	83
U30	Clock multiplier	125	58	61	62	67	65	73	72	85
U33	DC/DC Reg	125	59	61	62	67	66	72	74	85

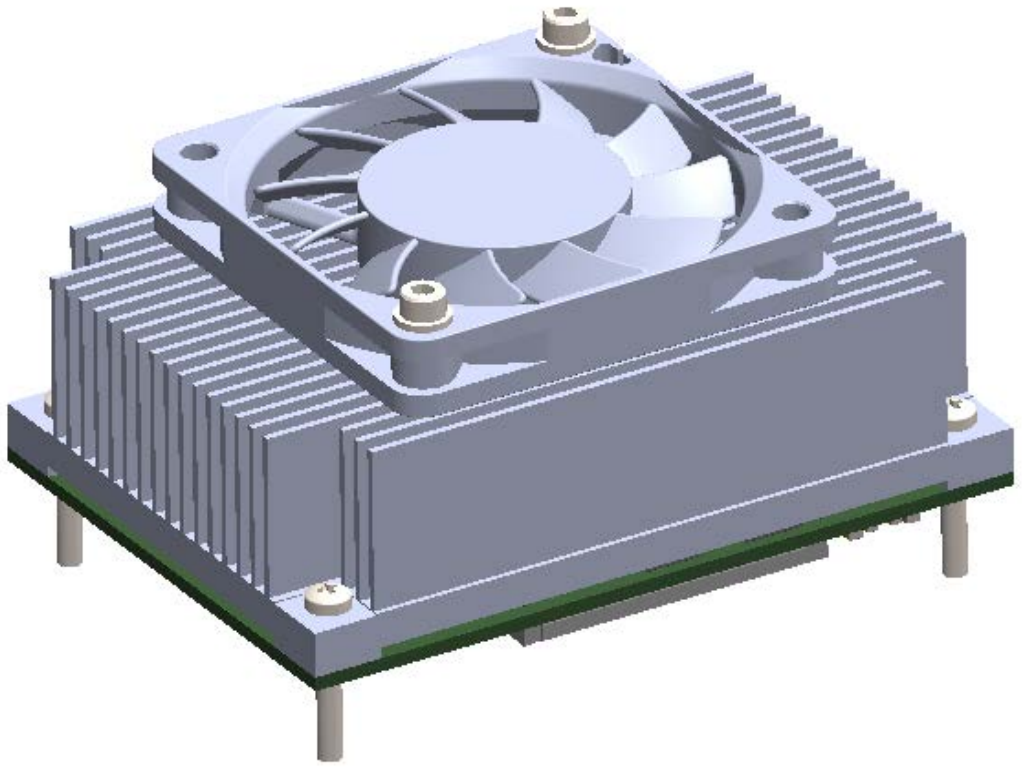


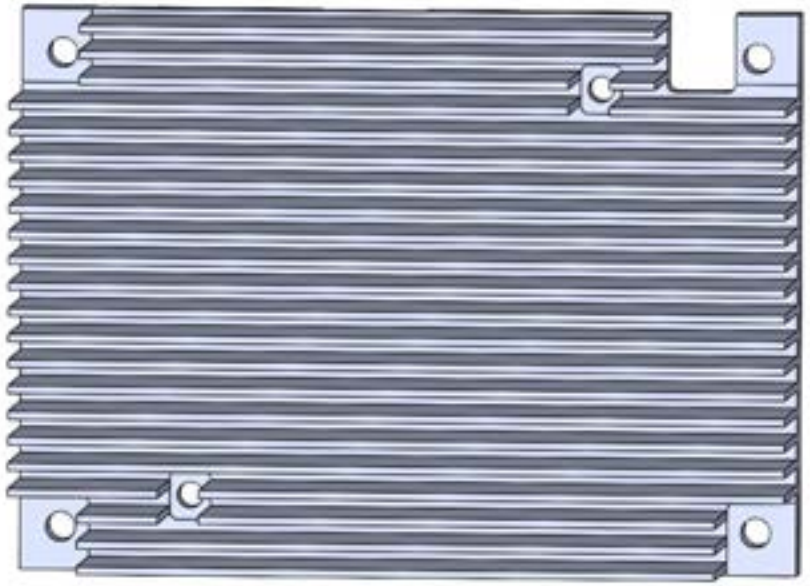
Board thermal simulations parameter with heatsink on SoC, PCB Edge and mounting holes – 85˚C

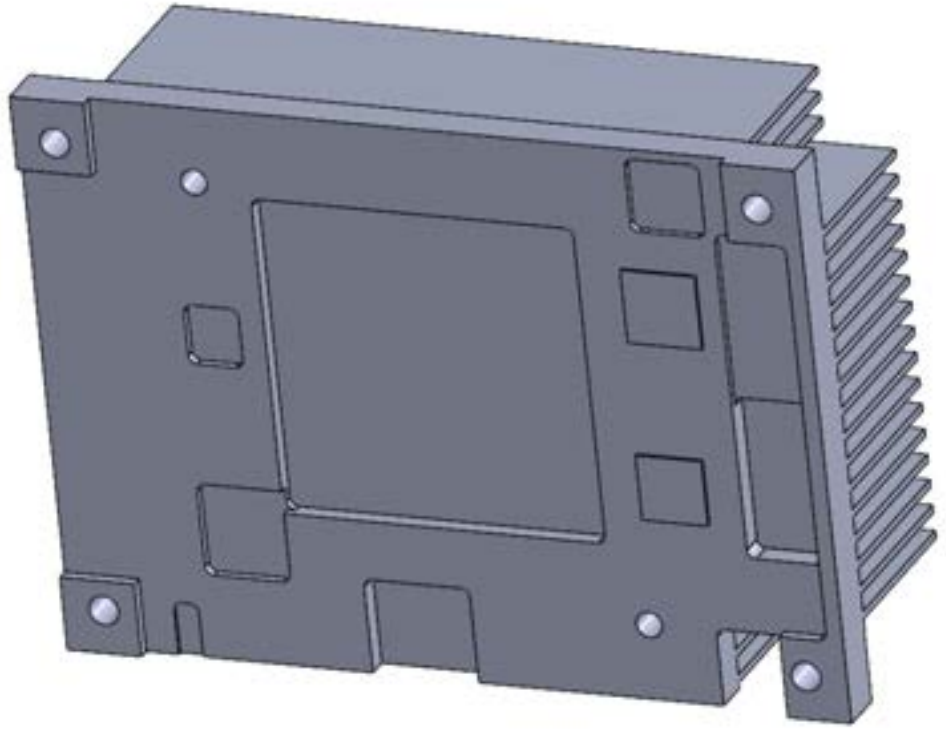
Simulated Component Temperatures

Component	Description	Temperature, °C				
		Max operating junction	Low power (10 W)	Lower nominal (20 W)	Nominal (29 W)	High power (50 W)
U1_c	FPGA case	85	89	93	96	104
U1_j	FPGA junction	100*	90	96	100	111
U8_j	DDR4 junction	100	89	92	95	102
U9_j	DDR4 junction	100	89	92	95	103
U10_j	DDR4 junction	100	89	92	96	103
U11_j	DDR4 junction	100	89	92	96	103
U12_j	DDR4 junction	100	89	92	96	104
U13_j	DC/DC Reg junction	125	94	102	110	129
U14_j	DC/DC Reg junction	125	92	100	107	122
U16_j	DC/DC Reg junction	125	93	101	108	125
U18_j	DC/DC Reg junction	125	91	96	102	114
U19_j	Ethernet Phy junction	125	91	96	101	113
U30_j	Clock multiplier junction	125	91	97	103	116
U33_j	DC/DC Reg junction	125	91	97	102	115

Custom Heatsink

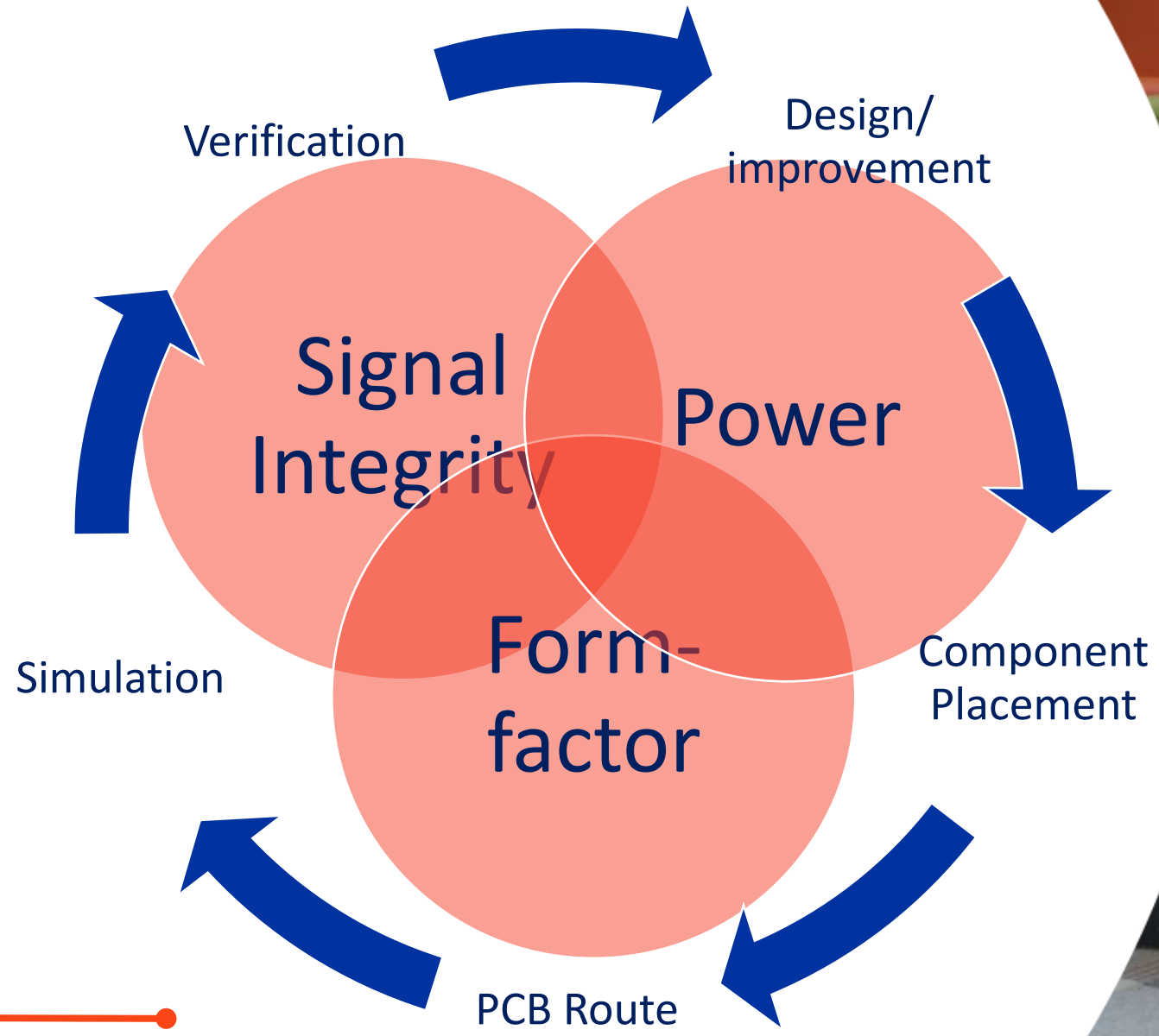


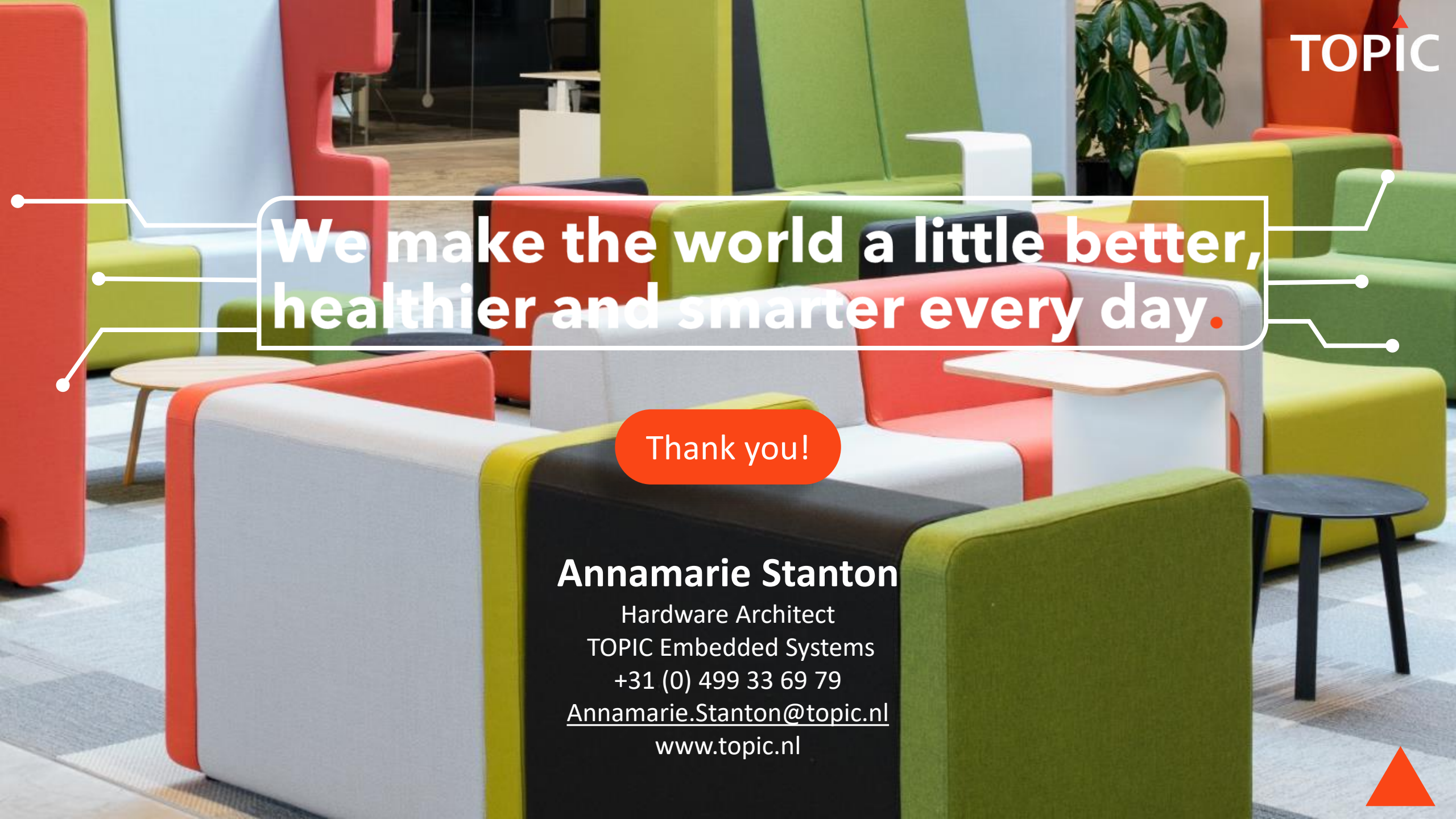




Conclusion

- Thermal design is an iterative process
- Thermal management cannot be designed in isolation
- Understand impact of Electronic design on Thermal management





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